

# Single-crystal Si formed on amorphous substrate at low temperature by nanopatterning and nickel-induced lateral crystallization

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Single-crystal silicon has been achieved by patterning amorphous silicon film on silicon dioxide substrate into nanoscale lines and nickel-induced lateral crystallization. Line width affects the single-crystal silicon formation significantly. Narrow line widths, 30 nm or less, resulted in little lateral crystallization; while for line widths above 250 nm, multiple grains started to form. *In-situ* transmission electron microscope observation has been used to study the crystallization process. Lithography-constrained single seeding is proposed to explain the single-crystal formation. © 2002 American Institute of Physics. [DOI: 10.1063/1.1498146]

Silicon-based thin film transistors (TFTs) on an amorphous substrate have many important applications, including active matrix liquid-crystal display (AMLCD) and future 3-dimensional (3D) integrated circuits.<sup>1-3</sup> However, silicon films deposited on amorphous substrate are typically in amorphous, microcrystalline, or polycrystalline states, which contain tremendous intrinsic defects, resulting in poor device performance and device-to-device nonuniformity. A single-crystal silicon film on amorphous substrate is highly desired but is difficult to achieve because single-crystal silicon cannot grow epitaxially on an amorphous substrate. Low temperature is also desired to lower the manufacturing cost and ensure the circuit integration.<sup>4</sup>

Many research efforts have been devoted to growing single-crystal silicon on amorphous substrate at low temperature. Excimer laser annealing has been a candidate to obtain this goal.<sup>1</sup> In this letter, we will report a different approach that can also achieve single-crystal silicon on amorphous substrate at low temperature. It is accomplished by nanopatterning of amorphous silicon ( $\alpha$ -Si) film followed by nickel-induced lateral crystallization (or NanoPAC).

Traditionally, nickel-induced lateral crystallization (Ni-ILC) has been used to crystallize  $\alpha$ -Si film at low temperature.<sup>5</sup> During the crystallization process, NiSi<sub>2</sub> precipitates are formed as heterogeneous nuclei for the solid phase crystallization of  $\alpha$ -Si before the spontaneous nucleation.<sup>6-8</sup> But the crystallized film is usually polycrystalline with longitudinal grains along the lateral crystallization direction.<sup>9</sup> By patterning the  $\alpha$ -Si film into lines before the lateral crystallization, however, we found that single-crystal Si can be achieved. The line width effects on the grain formation were studied. And *in-situ* transmission electron microscope (TEM) observation shows that nanopattern servers as a spatial constrain for single seed formation in the lateral crystallization.

The fabrication of NanoPAC process is as follows: 45

nm  $\alpha$ -Si film and a 10 nm SiO<sub>2</sub> mask layer were deposited on top of thermally oxidized silicon wafer by low pressure chemical vapor deposition at 550 °C, followed by plasma enhanced chemical vapor deposition (PECVD) at 250 °C. The  $\alpha$ -Si film was then patterned into lines by nanoimprint lithography,<sup>10</sup> liftoff, and reactive ion etching. The line length was 6 or 8  $\mu$ m. The line width varied from 20 to 450 nm. There was a large  $\alpha$ -Si pad at each end of the lines. After mask oxide removal and cleaning of the sample, another PECVD cap oxide layer was deposited to prevent stray Ni from contacting  $\alpha$ -Si line. Then a 1.5- $\mu$ m-wide window was opened at the center of the lines by photolithography and HF wet etch of cap oxide layer, followed by the deposition of 2.8 nm Ni by e-beam evaporation and a liftoff process. Finally, the patterned lines were crystallized at 500 °C by Ni-ILC for 10 h in nitrogen ambient. Figure 1 shows the schematic of NanoPAC crystallization. Patterned  $\alpha$ -Si lines without deposition of Ni were also annealed at the same time for comparison.

The lateral crystallization speed of unpatterned  $\alpha$ -Si film at 500 °C was measured as 0.85  $\mu$ m/h, which is close to the 1.25  $\mu$ m/h reported previously.<sup>11</sup> Annealed  $\alpha$ -Si lines were

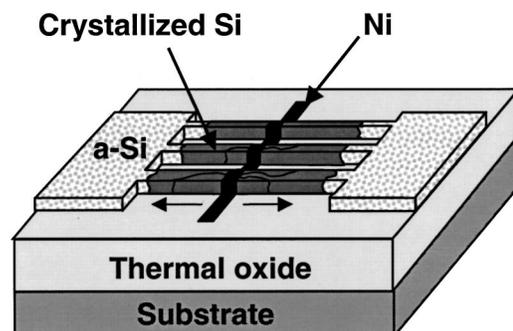


FIG. 1. Schematic of NanoPAC process:  $\alpha$ -Si film on thermally oxidized Si wafer is patterned into nanoscale lines and crystallized by Ni-ILC, (PECVD cap oxide is not shown for simplicity).

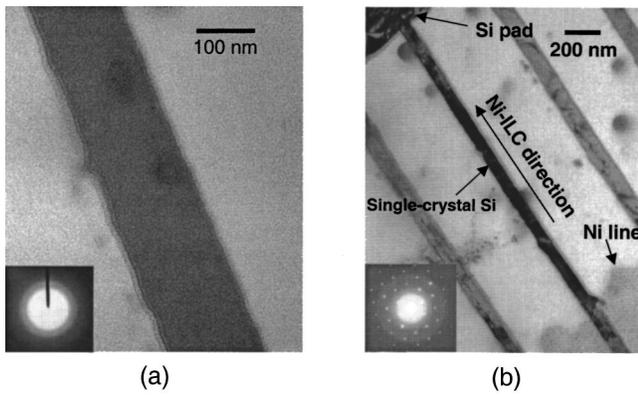


FIG. 2. (a) TEM image of an  $\alpha$ -Si line without Ni after 10 h annealing at 500 °C; (b) TEM image of single-crystal silicon crystallized from a 70-nm-wide  $\alpha$ -Si line by NanoPAC process at 500 °C for 10 h. Insets are the SAD patterns of the lines.

characterized using Philips CM20 and Philips CM200 TEMs.

The  $\alpha$ -Si lines without Ni deposition remained amorphous after 10 h annealing, as shown in Fig. 2(a). For  $\alpha$ -Si lines with Ni deposition, the single crystalline property of the lines was verified by comparing the convergent beam diffraction patterns (CBDPs) of the crystallized film along the line.

Transmission electron microscopy (TEM) study shows that single-crystal silicon has been formed inside the lines. Figure 2(b) shows a bright field image of a 70-nm-wide  $\alpha$ -Si line after the annealing. It is clearly seen that the  $\alpha$ -Si line was crystallized and formed single-crystal silicon with  $\langle 110 \rangle$  direction parallel to the beam direction, as shown by the inserted selective area diffraction (SAD) pattern. No grain boundary was observed. The crystallized silicon single crystal started from the initial lateral crystallization location and extended all the way to the silicon pad, with a length of 2.2  $\mu$ m. This length is limited by the lithographic layout we used instead of the NanoPAC process. Moreover, the location of the single crystal is completely determined by the lithographic layout, which is an important requirement for the fabrication of single grain TFTs.

TEM study also shows that the line width affects the silicon grain formation significantly. For lines with a narrow line width, 30 nm or less, the amorphous silicon lines could hardly be laterally crystallized after annealing, as shown in

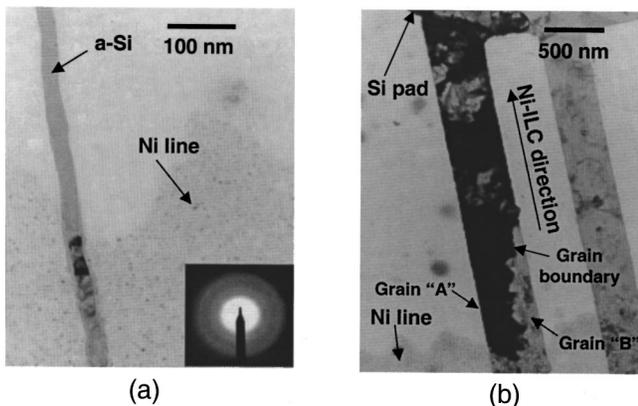


FIG. 3. Line width effects on the grain formation of NanoPAC process. (a) TEM image of a 20-nm-wide line, inserted diffraction pattern shows the amorphous state of the line; (b) TEM image of a 450-nm-wide line with competitive grain growth at beginning of the lateral crystallization.

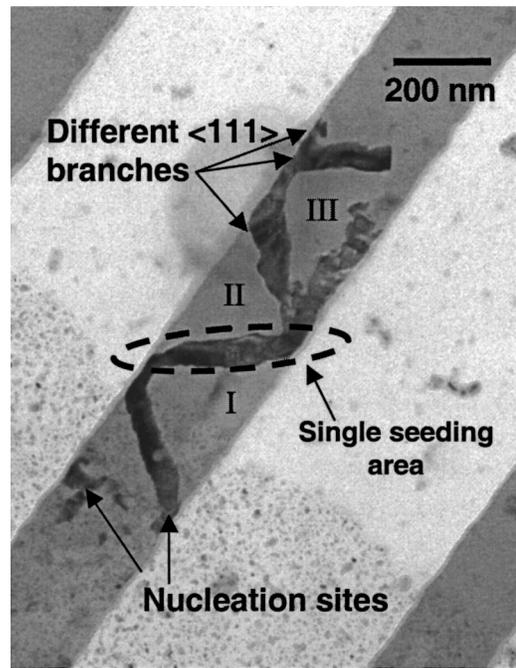


FIG. 4. TEM image of a 250-nm-wide line shows lithography-constrained single seeding in NanoPAC process: the  $\alpha$ -Si beyond the single seeding area can only be seeded by the single seeding grain before the spontaneous nucleation.

Fig. 3(a). The amorphous state of the lines was confirmed by tilting the sample to check grain boundaries under TEM as well as by the SAD pattern. On the other hand, the  $\alpha$ -Si line in contact with Ni was crystallized into polycrystalline silicon, which means the  $\text{NiSi}_2$  precipitates were still formed. The absence of the lateral crystallization in the narrow line is not well understood yet and could be related to the stress generated in the narrow  $\alpha$ -Si lines upon crystallization that could stall the crystallization process.<sup>12</sup>

Moreover, for lines with a wider line width, 250 nm and above, single-crystal silicon can still form. However, competitive grain growth could happen at the beginning of the lateral crystallization. Figure 3(b) clearly shows that two grains, labeled A and B, were initiated at the edge of deposited Ni in a 450-nm-wide  $\alpha$ -Si line, as labeled in the figure. The black and white contrast between the two grains is due to the diffractions of electron beam by the different crystalline orientations of the grains, therefore shows the shape of the two grains. After 1  $\mu$ m lateral growth, grain A dominated in the grain growth and the grain boundary was terminated at the sidewall of the  $\alpha$ -Si line.

The phenomenon of pattern as a grain boundary filter, as shown in the 450-nm-wide line, was demonstrated previously in solid phase epitaxy of germanium<sup>13</sup> to obtain large-grained semiconductors. However, the single-crystal formation without grain boundaries outside the heterogeneous nucleation area [Fig. 2(b), the 70-nm-wide line] has never been reported.

To understand the merits of nanopattern on the single-crystal formation, *in-situ* TEM observation has been used to study the detailed crystallization mechanism within a pattern. Figure 4 shows a TEM picture of a 250-nm-wide  $\alpha$ -Si line after *in-situ* annealing with a hot stage at 700 °C for 30 mins. The real temperature at the sample area is not known and

should be lower than that of the hot stage because the  $\alpha$ -Si line is on a  $\text{SiO}_2$  membrane, which is a good heat insulator. We can see that two nuclei were formed close to the edge of the heterogeneous nucleation area. One nucleus had the chance to grow rapidly into the Ni-free area before the other one. The grain has a needle shape along  $\langle 111 \rangle$  direction because  $\langle 111 \rangle$  surface of the  $\text{NiSi}_2$  serves as a template for the solid phase epitaxy of  $\alpha$ -Si.<sup>6-8</sup> When the crystallization front reaches sidewall of the pattern, it changes the direction to either along the sidewall or along other  $\langle 111 \rangle$  directions to form a needle network. And the narrow pattern serves as a spatial confinement so that one grain can easily grow across the width of the pattern before other grains' arrival. Once one branch of the grain network dominates the cross section of the pattern outside the heterogeneous nucleation area, other orientations from the heterogeneous nucleation area will be prohibited, and the grain becomes the only seed for the lateral crystallization (the single seeding area in Fig. 4). We call it lithography-constrained single seeding in the NanoPAC process. Finally, the  $\alpha$ -Si film beyond the single seeding area (such as regions II and III) can be crystallized by more  $\langle 111 \rangle$  crystallization fronts developed from the single seeding grain to form single-crystal silicon.<sup>14</sup> The  $\alpha$ -Si before the single seeding area (region I) could be crystallized by the single seeding grain or by other grains from the heterogeneous nucleation area to show competitive grain growth.

In summary, by combining nanopatterning and Ni-ILC, single-crystal silicon has been formed on amorphous substrate at low temperature. Line width affects the grain formation significantly. *In-situ* TEM has been used to study the crystallization process within patterned  $\alpha$ -Si lines. Lithography-constrained single seeding has been proposed to explain the single-crystal silicon formation. The crystallized single-crystal Si could be designed as the channel region of the devices for the fabrication of high performance TFTs on

glassy substrate, as well as for high performance, low power 3D integrated circuits.<sup>15</sup> The optimum line width of forming single-crystal Si has also been studied and found to be from 50 to 200 nm.<sup>16</sup>

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- <sup>1</sup>James S. Im, Robert S. Sposili, and M. A. Crowder, Appl. Phys. Lett. **70**, 3434 (1997).
- <sup>2</sup>M. A. Crowder, P. G. Carey, P. M. Smith, Robert S. Sposili, Hans S. Cho, and James S. Im, IEEE Electron Device Lett. **19**, 306 (1998).
- <sup>3</sup>V. Subramanian and K. C. Saraswat, IEEE Trans. Electron Devices **45**, 1934 (1998).
- <sup>4</sup>In AMLCD application, glass substrate is usually used, which has a strain point around 600 °C; for 3D integrated circuits application, substrate temperature below 850 °C is often wanted to ensure the stableness of underlying devices.
- <sup>5</sup>S.-W. Lee and S.-K. Joo, IEEE Electron Device Lett. **17**, 160 (1996).
- <sup>6</sup>R. C. Cammarata, C. V. Thompson, C. Hayzelden, and K. N. Tu, J. Mater. Res. **5**, 2133 (1990).
- <sup>7</sup>C. Hayzelden, J. L. Batstone, and R. C. Cammarata, Appl. Phys. Lett. **60**, 225 (1992).
- <sup>8</sup>C. Hayzelden and J. L. Batstone, J. Appl. Phys. **73**, 8279 (1993).
- <sup>9</sup>G. A. Bhat, Z. Jin, H. S. Kwok, and M. Wong, IEEE Electron Device Lett. **20**, 97 (1999).
- <sup>10</sup>S. Y. Chou, P. R. Krauss, and P. J. Renstrom, Science **272**, 85 (1996).
- <sup>11</sup>H. Kim, J. G. Couillard, and D. G. Ast, Appl. Phys. Lett. **72**, 803 (1998).
- <sup>12</sup>X. Bo, N. Yao, and J. C. Sturm, Mat. Res. Soc. Symp. Proc. **715**, A16.4 (2002).
- <sup>13</sup>H. Tanabe, C. M. Chen, and H. A. Atwater, Appl. Phys. Lett. **77**, 4325 (2000).
- <sup>14</sup>J. Gu, N. Yao, H. Zandbergen, J. K. Farrer and S. Y. Chou, 2002 MRS Spring Meeting, San Francisco, California, 2002 (unpublished).
- <sup>15</sup>V. W. C. Chan, P. C. H. Chan, and M. Chan, IEEE Electron Device Lett. **22**, 77 (2001).
- <sup>16</sup>J. Gu, S. Y. Chou, and H. Zandbergen, 43rd Electronic Materials Conference, Notre Dame, Indiana, 2001 (unpublished).